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Patent
Case No.: 10200-88
Client Ref.: PM00027

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

Sundar Narayanan

Appl. No.: 09/753,011

Filed: January 2, 2001

For: METHOD OF MAKING UNIFORM OXIDE LAYER

Group Art Unit: 2812

Examiner: J. Jones

Assistant Commissioner of Patents
Washington, D.C. 20231

RESPONSE

Dear Sir:

This responds to the outstanding Office Action mailed October 3, 2001. In view of the following Amendments and Remarks, Applicants believe the application is in condition for allowance and request the same.

AMENDMENT

In accordance with Rule 1.121, a clean copy of the amended claims and new claims is reproduced below. An Appendix is attached to show the changes made to the claims by current amendment.

In the Drawings:

Figures 1-5 have been amended to show that the isolation technique illustrated is conventional. Amendments are made in red.

In the Claims:

Please cancel claim 20 and amend claims 1, 12, and 21 as follows:

A1

1. (Amended) A method of forming a semiconductor structure, comprising:
forming an isolation region in a semiconductor substrate; wherein
a first oxide layer is on said substrate,
a first sacrificial layer is on said first oxide layer, wherein said first sacrificial layer comprises an oxide, and
a first nitride layer is on said first sacrificial layer.

A2

12. (Amended) A method of forming a semiconductor structure, comprising:
removing a first nitride layer and a first sacrificial layer, wherein said first sacrificial layer comprises an oxide;
wherein a first oxide layer is on a substrate,
said first sacrificial layer is on said first oxide layer, and
said first nitride layer is on said first sacrificial layer.

A3

21. (Amended) In a method of forming an isolation region in a semiconductor device, including forming an isolation nitride on a substrate, the improvement comprising forming a first sacrificial layer between said isolation nitride

A3 cont'd

and said substrate and forming a second sacrificial layer between said first sacrificial layer and said substrate.

Please add the following new claim.

A4

23. The method of claim 3, wherein said forming an isolation region comprises depositing an oxide onto said first nitride layer and into a trench adjacent to said first nitride layer, said first sacrificial layer, and said first oxide layer.

REMARKS

Claims 1-19 and 21-23 are pending. Claim 20 is cancelled. Claims 1, 12, and 21 are amended. Claim 23 is new.

Claims 2-11, 14-19, and 21-22 were considered allowable if rewritten in independent form. Claim 21 has been rewritten in independent form, as suggested, and claim 20 has been deleted.

The amendments to claims 1 and 12 are supported by original claim 3, and the specification, Page 3, Lines 1-6. Original claim 1 and Figure 8 support new claim 23. In view of the following amendments and remarks, Applicants respectfully request reconsideration of the application.

Claims 1–2 and 12–13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. 10–289990 (hereinafter referred to as "*Heisei*"). The rejection was based on the reference's teaching of a layer between a first oxide layer and a nitride layer. Applicants respectfully traverse.

Heisei teaches a semiconductor device equipped with flash memory. Initially, the device consists of five layers: a bottom substrate (10), a tunnel oxide (21), a polycrystalline silicon conductive layer (22), a polycrystalline silicon pad oxide (23), and a silicon nitride top layer (24). It is clear from paragraph [0044] of the reference that layers (21) and (22) (which are protected by resist (52)) remain in the finished device. If this were not the case, a memory device could not be formed because there would be no conductive layer (22).

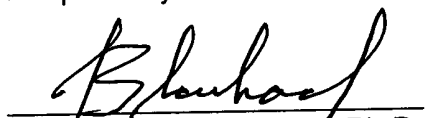
Unlike the device of *Heisei*, the claimed invention initially includes a substrate (102), a screen oxide (110), at least one sacrificial layer (118/120) comprising an oxide, and a nitride layer (106).

Layer (22) from *Heisei*, is a conductive layer made from polycrystalline silicon, while layer (118) of the claimed invention is a first sacrificial layer comprising an oxide. The conductive, polycrystalline silicon layer of *Heisei* does not teach a sacrificial layer comprising an oxide. *Heisei* does not teach the sacrificial oxide layer of the claims; only a polycrystalline silicon layer lying between the screen oxide and the nitride layer. *Heisei* does not anticipate the independent claims.

Conclusion

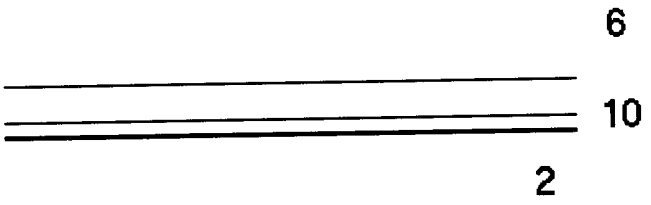
Applicants have overcome each of the rejections. The application is therefore in condition for allowance and early notification of allowance is respectfully requested. If, for any reason, the Examiner believes that the amendments and remarks do not put the claims in condition for allowance, the undersigned attorney can be reached at (312) 321-4898 to resolve any remaining issues.

Respectfully submitted,



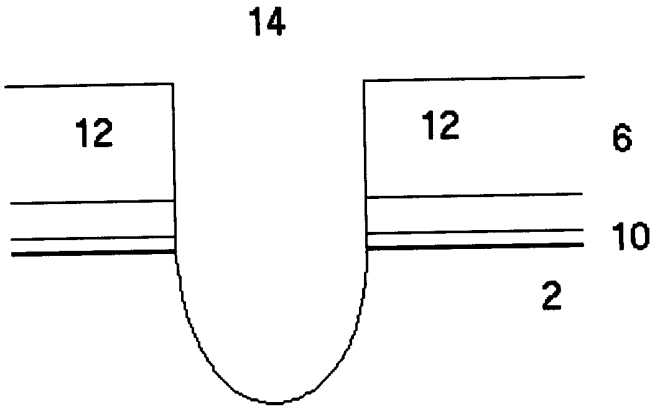
Jonathan M. Blanchard, Ph.D.
Reg. No. 48,927
Attorney for Applicants

BRINKS HOFER
GILSON & LIONE
P.O. Box 10395
Chicago, IL 60610
(312) 321-4200



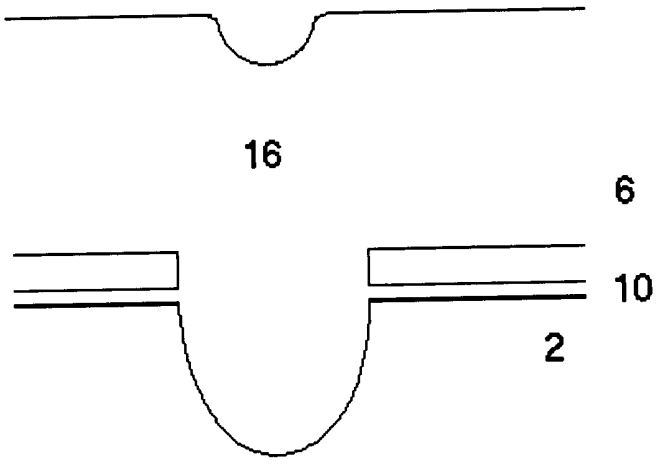
Conventional

Figure 1



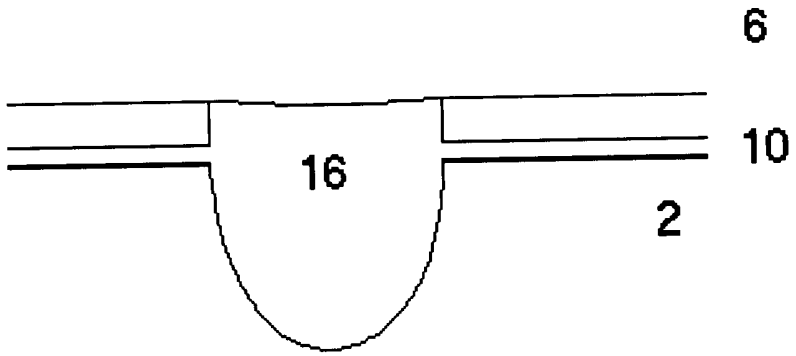
Conventional

Figure 2



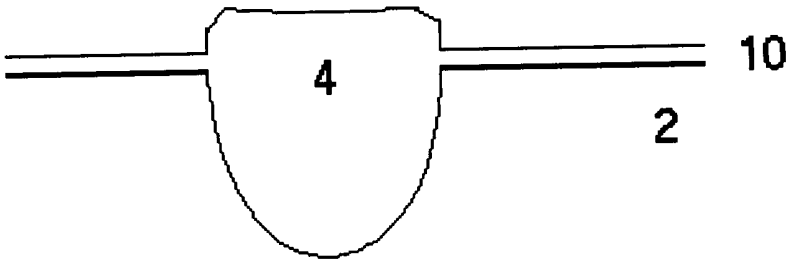
Conventional

Figure 3



Conventional

Figure 4



Conventional

Figure 5